

## CLAIMS

1. A semiconductor memory comprising:

a plurality of memory arrays, each of which comprises a plurality of memory cells arranged in a matrix and controlled by a row address counter uniquely assigned to each of said memory arrays, said row address counter generating a first word address; and

means for enabling a refresh operation in said memory cells, said memory cells being identified by said first word address when a refresh command is issued to a corresponding memory array.

2. The semiconductor memory as recited in claim 1, wherein each of said memory arrays further comprises a second word address common to at least two of said memory arrays, and wherein an enabling means enables a memory access operation in said memory cells, said memory cells being identified by said second word address when a memory access command is issued to a corresponding memory array.

3. The semiconductor memory as recited in claim 2, wherein said refresh command is provided by a refresh bank select signal to a corresponding memory array.

4. The semiconductor memory as recited in claim 1, wherein said first address is updated when said refresh operation has been completed, by incrementing said row address counter.

5. The semiconductor memory as recited in claim 3, wherein said memory access command is provided by a bank select signal to a corresponding memory array.

6. The semiconductor memory as recited in claim 5, wherein said refresh bank select signal enables a refresh operation in said first memory array while concurrently enabling a memory access operation in said second memory array.
7. The semiconductor memory as recited in claim 6, wherein said refresh bank select signal enables a refresh operation in at least one additional memory array while concurrently enabling a memory refresh operation in said first memory array and a memory access operation in said second memory array.
8. The semiconductor memory as recited in claim 6, wherein each of said plurality of the memory arrays further comprises switching means for selectively coupling said first and said second word address to row decoders within said memory array, and wherein a refresh operation is controlled by said first word address, and a memory access operation is controlled by the second word addresses.
9. The semiconductor memory as recited in claim 8, wherein each of said memory arrays further comprises word address latches, said word address latches being coupled to said switching means, and wherein said third memory array initiates a memory access operation when the corresponding bank select signal is provided to said third memory array without waiting for the completion of:
- a) said refresh operation in said first memory array, and
  - b) said memory access operation in said second memory array.
10. The semiconductor memory as recited in claim 9, wherein a fourth memory array initiates a memory refresh operation when a corresponding refresh bank select signal is provided to said fourth memory array without waiting for the completion of:
- a) said refresh operation in said first memory array, and

b) said memory access operation in said second memory array, while concurrently initiating a memory access operation in said third memory array.

11. The semiconductor memory as recited in claim 10, wherein said refresh bank select signal enables a refresh operation in at least one additional memory array, while concurrently enabling a memory refresh operation in said first memory array and a memory access operation in said second memory array.

12. The semiconductor memory as recited in claim 11, wherein said refresh bank select signal enables a refresh operation in at least one additional memory array, while concurrently enabling a memory refresh operation in said fourth memory array and a memory access operation in said third memory array.

13. The semiconductor memory as recited in claim 5, wherein said refresh bank select signal and said memory access bank select signal are independent of each other.

14. The semiconductor memory as recited in claim 7, wherein said refresh bank, said memory access bank, and said at least one more refresh backs are distinct from each other.

15. The semiconductor memory as recited in claim 10, wherein the time interval for activating one of said memory arrays to perform either a refresh operation or a bank access operation is longer than the random access cycle time.

16. The semiconductor memory as recited in claim 15, wherein the time interval for activating at least two memory arrays to perform either a refresh operation or a bank access operation is shorter than the random access cycle time.

17. A semiconductor memory comprising:

a plurality of memory arrays, each of said memory arrays comprising a plurality of memory cells arranged in a matrix and controlled by a row address counter uniquely assigned to each of said each memory arrays, said row address counter generating a first word address;

means enabling a refresh operation in said memory cells, wherein said memory cells are identified by the first word address when a refresh command is provided to a corresponding memory array;

a common second address coupling at least two memory arrays;

means for selectively coupling said first and said second word addresses to row decoders within each of said memory arrays, wherein

a refresh operation is enabled by said first word address in a first memory array while enabling a memory access operation by said second word address in a second memory array.

18. The semiconductor memory as recited in claim 17, wherein said first address is updated when said refresh operation is completed by incrementing said row address counter.